a second external line provided outside the semiconductor integrated circuit and adapted to be connected to the first internal line;

a first connection for connecting the first external line and the first internal terminal;

a second connection for connecting the first external line and the second internal terminal;

a third connection for connecting the second external line and the third internal terminal;

a first switch connected between the first internal terminal and the first internal line; and

a second switch connected between the second internal terminal and the first internal line.

44. (Once Amended) A method for inspecting a semiconductor device comprising: a first internal line provided within the semiconductor integrated circuit; a first internal terminal, a second internal terminal, and a third internal terminal provided within the semiconductor integrated circuit; a first external line provided outside the semiconductor integrated circuit; a second external line provided outside the semiconductor integrated circuit and adapted to be connected to the first internal line; a first connection for connecting the first external line and the first internal terminal; a second connection for connecting the first external line and the second internal terminal; a third connection for connecting the second external line and the third internal terminal; a first switch connected between the first internal terminal and the first internal line; and a second switch connected between the second internal terminal and the first internal line, which method comprises:

closing the first switch while opening the second switch;

applying an inspection signal from the first external line to the second external line; and

inspecting a connection state between the first external line and the first internal terminal at the first connection.

Please add new claims 49-66 as follows.

49. (New) The semiconductor device according to claim 20, wherein the second external line is connected to the first internal line without passing through a switch.

50. (New) The semiconductor device according to claim 49, wherein the second external line is directly connected to the first internal line.

51. (New) The semiconductor device according to claim 49, further comprising a switch controlling section within the semiconductor integrated circuit for controlling opening and closing of the first and second switches.

52. (New) The semiconductor device according to claim 20, further comprising a third switch connected between the third internal terminal and the first internal line.

53. (New) The semiconductor device according to claim 52, further comprising a switch controlling section within the semiconductor integrated circuit for controlling opening and closing of the first, second, and third switches.

54. (New) The semiconductor device according to claim 53, wherein:

a power source terminal of the switch controlling section is connected to an internal power source line connected to a power source line provided outside the semiconductor integrated circuit;

a grounding terminal of the switch controlling section is connected to an internal grounding line connected to a grounding line provided outside the semiconductor integrated circuit; and

at least one of the internal power source line and the internal grounding line is separated from the first internal line.

55. (New) The semiconductor device according to claim 53, wherein:

a power source terminal of the switch controlling section is connected to an internal power source line connected to a power source line provided outside the semiconductor integrated circuit; and

a grounding terminal of the switch controlling section is connected to the third internal terminal.

56. (New) The semiconductor device according to claim 53, wherein:

a grounding terminal of the switch controlling section is connected to an internal grounding line connected to a grounding line provided outside the semiconductor integrated circuit, and

a power source terminal of the switch controlling section is connected to the third internal terminal.

57. (New) The semiconductor device according to claim 52, wherein the third switch is configured to always be on.

58. (New) The semiconductor device according to claim 57, further comprising a switch controlling section within the semiconductor integrated circuit for controlling opening and closing of the first, second, and third switches.

59. (New) The semiconductor device according to claim 52, further comprising a switch controlling section within the semiconductor integrated circuit for controlling opening and closing of the first and second switches.

60. (New) The method according to claim 44, further comprising a third switch connected between the third internal terminal and the first internal line.

61. (New) The method according to claim 60, further comprising a switch controlling section within the semiconductor integrated circuit for controlling opening and closing of the first, second, and third switches.

62. (New) The method according to claim 61, wherein:

a power source terminal of the switch controlling section is connected to an internal power source line connected to a power source line provided outside the semiconductor integrated circuit;

a grounding terminal of the switch controlling section is connected to an internal grounding line connected to a grounding line provided outside the semiconductor integrated circuit; and

at least one of the internal power source line and the internal grounding line is separated from the first internal line.

63. (New) The method according to claim 61, wherein:

a power source terminal of the switch controlling section is connected to an internal power source line connected to a power source line provided outside the semiconductor integrated circuit; and

a grounding terminal of the switch controlling section is connected to the third internal terminal.

64. (New) The method according to claim 61, wherein:

a grounding terminal of the switch controlling section is connected to an internal grounding line connected to a grounding line provided outside the semiconductor integrated circuit, and

a power source terminal of the switch controlling section is connected to the third internal terminal.

65. (New) A semiconductor device having a semiconductor integrated circuit, the semiconductor device comprising:

an internal line provided within the semiconductor integrated circuit;

a first internal terminal, a second internal terminal, and a third internal terminal provided within the semiconductor integrated circuit;

a first connection adapted for connecting an external line and the first internal terminal;

a second connection adapted for connecting an external line and the second internal terminal;

a third connection adapted for connecting an external line and the third internal terminal;

a first switch connected between the first internal terminal and the internal line; and

a second switch connected between the second internal terminal and the internal line.

66. The semiconductor device according to claim 65, further comprising a switch controlling section within the semiconductor integrated circuit for controlling opening and closing of the first and second switches.